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PTO/SB/08A (08-00)



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**Substitute for form 1449A/PTO**

## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of

Substitute for form 1449A/PTO		<b>Compl te if Known</b>		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>		Application Number	10/628,737	
		Filing Date	July 28, 2003	
		First Named Inventor	PEIYI ZHAO	
		Group Art Unit	Not Assigned 2916	
		Examiner Name	Not Assigned M. N. M. M. M.	
Sheet	1	of	1	Attorney Docket Number
				17220-6

## **U.S. PATENT DOCUMENTS**

## **FOREIGN PATENT DOCUMENTS**

Examiner Signature	<u>WML</u>	Date Considered	12/9/14
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Unique citation designation number. <sup>2</sup> See attached Kinds of U.S. Patent Documents. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

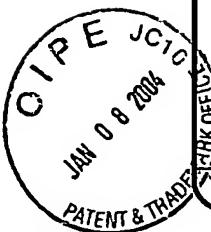
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PTO/SB/088 (08-00)  
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet

1

of

1

C mpt if Kn wn

Application Number	10/628,737
Filing Date	July 28, 2003
First Named Inventor	PBIYI ZHAO
Group Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	17220-6

### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
M	1	SEONGMOO HEO, RONNY KRASHINSKY, AND KRSTE ASANOVIE, Activity-Sensitive Flip-Flop and Latch Selection for Reduced Energy, 19th Conference on Advanced Research in VLSI, Salt Lake City, UT, March 2001	
M	2	HIROSHI KAWAGUCHI and TAKAYASU SAKURAI, A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction, IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998.	
M	3	SEONGMOO HEO and KRSTE ASANOVIE, Load-Sensitive Flip-Flop Characterization, IEEE Journal of Solid-State Circuits, 2001 ✓	
M	4	BAI-SUN KONG, SAM-SOO KIM, and YOUNG-HYUN JUN, Conditional-Capture Flip-Flop for Statistical Power Reduction, IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001.	
M	5	JIREN YUAN and CHRISTER SVENSSON, High-Speed CMOS Circuit Technique, IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989. ✓	
M	6	RABAEE, J.M.: Digital Integrated Circuits, Chapter 7, "Designing Sequential Logic Circuits", University of California, Berkeley, 2000. ✓	
M	7	VLADIMIR STOJANOVIC and VOJIN G. OKLOBDZIJA, Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems, IEEE Journal of Solid-State Circuits, Vol.34, No. 4, April 1999.	
M	8	J. TSCHANZ, et al., Comparative Delay and Energy of Sgl. Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for Hi-Performance Microprocessors Intn'l Symp. on Low Power Elect and Design, Pp(s): 147-152, 2001. ✓	

Examiner Signature

Date Considered

1/9/02

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